In the Claims:

1. (original) A semiconductor memory comprising:

an array of first memory elements including bit lines coupled with corresponding columns of elements in the array and word lines coupled with corresponding rows of elements in the array, each of the first memory elements holding data, said array further including a security row of second memory elements coupled to a corresponding security word line, each of the second memory elements being coupled to the bit lines of the array of first memory elements, said second memory elements being programmed in a first mode of operation to allow the data in the first memory elements to be read, said second memory elements being programmed in a second mode of operation to prevent the data in the first memory elements from being read; and

means for selecting the security row to operate in either the first mode of operation or the second mode of operation.

2. (original) The semiconductor memory of claim 1 wherein the security row is selected for read when an external read command is requested and deselected when an internal read command is requested.

3. (original) The method of claim 1 wherein the second mode of operation includes returning a default zero value in response to an external read request of said memory.

4. (original) The semiconductor memory of claim 1 wherein the means for selecting includes a chip erase command to program the second memory elements to operate in the first mode of operation.

5. (original) The semiconductor memory of claim 1 wherein the means for selecting includes a write lockbit command to program the second memory elements to operate in the second mode of operation.

6. (original) The semiconductor memory of claim 1 further including a security row of third memory elements coupled to a corresponding security bit line, each of the third memory elements coupled to the word lines of the array of the second memory elements, said third memory elements being programmed in a first mode of operation to allow the data in the first memory elements to be read, said third memory elements being programmed in a second mode of operation to prevent the data in the first memory elements from being read.

7. (original) The semiconductor memory of claim 6 further comprising means for erasing of the first memory elements followed the second and third memory elements such that the previous data contents are destroyed before the second and third memory elements operate in the first mode of operation.

8. (original) The semiconductor memory of claim 6 wherein the security row of third memory elements is selected for reading at appropriate times so as to determine a mode of operation of the third memory elements.

9. (original) The semiconductor memory of claim 1 further comprising a plurality of security rows distributed across the array.

10. (currently amended) A method of operating an embedded semiconductor memory comprising:

having security lock protection responsive to an external access request to said memory; and

disabling external access to a memory array row whenever a security bit in ~~the~~ a security row indicates a locked status, and otherwise enabling access to the memory array.

11. (original) The method of claim 10 wherein internal access is enabled regardless of locked/unlocked status.

12. (original) The method of claim 10 further comprising erasing memory contents of said memory prior to resetting security row memory cell elements and lock bit cells to an unlocked status.

13. (original) The method of claim 10 wherein a chip erase command erases and unlocks all security bits at the same rate and in the same manner as all elements in the memory array are erased.

14. (currently amended) The method of claim 10 wherein ~~said~~ a lockbit sense amplifier is selected to detect and latch the locked or unlocked status of the lockbit cells.